High Peak Pulse Power Silicon Double-Drift IMPATT Diodes

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Abstract—**The performance of high peak pulse power silicon double-drift IMPATT devices operated at medium pulse repetition frequency are discussed. Several devices were characterized and achieved more than 45-W peak pulse power with 10-percent duty cycle at 9.7 GHz. Conversion efficiencies in the order of 9.7–11.2 percent were observed. These results compare with previously reported 19-W peak power, 10-percent duty-cycle, and 9.5-percent efficiency [2].**

I. Introduction

HIGH-POWER solid-state pulsed microwave (*X*-band) sources are needed for use in airborne radar systems. Power combiners are being designed to increase the overall output power by using a large number of devices. By increasing the power of the individual devices, the number of diodes required per combiner can be reduced. Current results indicate that a silicon double-drift IMPATT device can produce approximately two times the power (>40 W) of the presently commercially available diodes (19 W) [2] and still maintain an efficiency of >9.0 percent.

The design criteria and performance of an *X*-band high peak power silicon double-drift IMPATT diode are described in this paper.

II. Device Consideration

The structure used is a silicon double-drift p^+-p-n-n^+ device [1] optimized for high peak power. Current densities are in the order of 1.5–1.6 kA/cm^2. A large area design ($A = 1.6 \times 10^{-3}$ cm^2) was used to reduce the thermal resistance and increase the power out. This area is twice the area of earlier designs. Although efficiencies have been reported to be degraded for large area devices [3], experiments have shown that compensation can be made in the doping density and layer width to yield higher efficiencies for areas as large as eight times the area of a comparable CW device. Hierl *et al.* [4] and Wallace *et al.* [5] have also shown that efficiency decreases with increasing area for high-power GaAs IMPATT's without reoptimization for a given area. Lot #2 of the present work has shown efficiencies greater than 10 percent which is comparable to the earlier designs (10–12 percent).

The large junction area increases the Q of the device and lowers the negative resistance. This lower negative resistance ($\simeq 1\ \Omega$ at full power) increases the importance of losses in the immediate vicinity of the chip's active area (metal contact, bond wire, package, cavity, etc.).

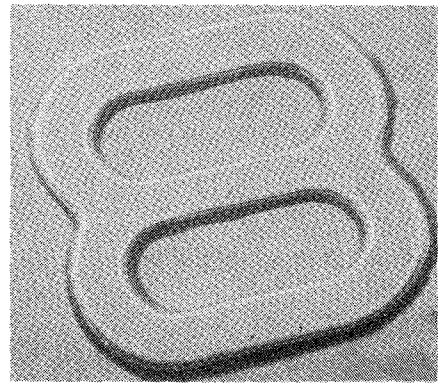

Fig. 1. SEM photograph of diode chip.

There are two major ways of reducing the thermal resistance of a device: 1) lower thermal resistance heat-sink material (diamond), 2) geometrical designs. The present device takes advantage of the latter by using a figure 8 on a plated heat-sink structure (see Fig. 1). The thermal resistance (typically 5°C/W) is considerably lower than is possible with a large dot or annular ring structure. Also the avalanche breakdown and current density is more uniform.

III. Microwave Results

Two lots were evaluated for microwave performance. The highest peak pulse power observed was 49 W at 10-percent duty cycle, 400-ns pulsewidth, 232°C average junction temperature rise,[1] and 9.4-percent efficiency. After passing the 45-W level, the efficiency degraded, and the temperature increased rapidly.

The circuit used is a coaxial single transformer with two to three tuning screws placed in front for fine tuning. The minimal variation in detected RF power versus time is shown in Fig. 2. A single uniform frequency chirp of about 90 MHz was achieved with pulsewidths of up to 3.5 μs. It is necessary to compensate for the changing impedance during the pulse if the pulsewidth exceeds 1–2 μs. These longer pulses need a locking signal if a single frequency is required. Fig. 2 reveals the change in operating voltage during a 3.5-μs pulse for a constant operating current of 2 A. Most of the voltage change from the

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[1]The average rise in the junction temperature above the ambient temperature is taken as the average dissipated power times the thermal impedance.

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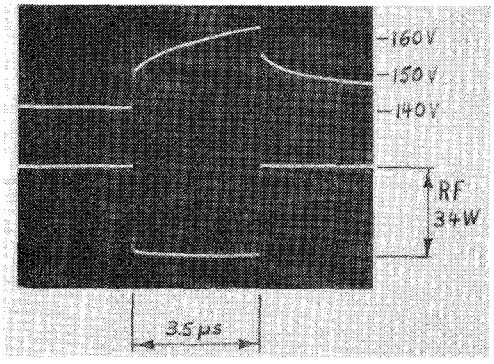

Fig. 2. Operating voltage and detected RF output power against time at 9.7 GHz, 3.5-μs pulsewidth, and 10-percent duty cycle.

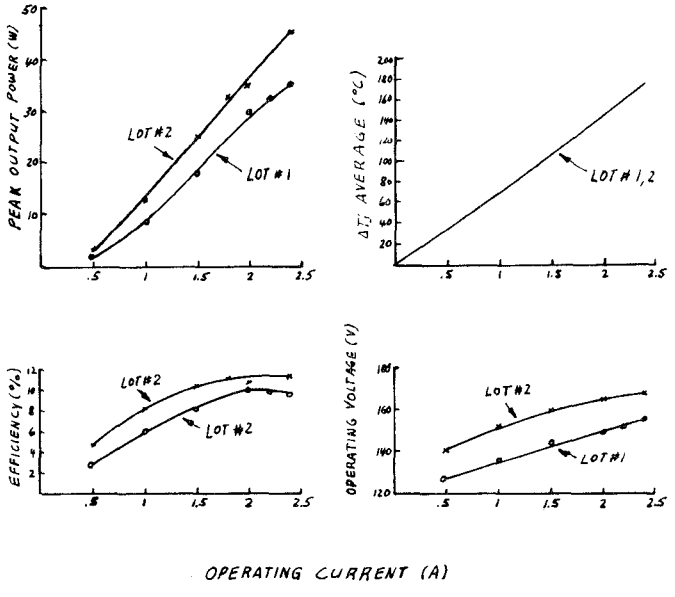

Fig. 3. (a) Pulsed power output, (b) average junction temperature rise, (c) efficiency, and (d) operating voltage versus current for 1-μs pulsewidth and 10-percent duty cycle.

beginning to the end of the pulse is due to heat; some change in the impedance is, therefore, noticeable during the pulse.

It is useful to a designer to know as much as possible about the operating conditions of a device. Fig. 3 illustrates the relationship between peak output power, efficiency, average junction temperature rise, operating voltage, and pulsed operating current. The bias pulsewidth was fixed at 1 μs with a duty cycle of 10 percent. The circuit load resistance was adjusted to result in maximum output power at each value of bias current. Several significant operating characteristics are presented in Fig. 3. Note that there is an almost linear relationship between both output power and average temperature rise with operating current. Lots #1 and 2 are tracking each other on the temperature curve. Operating voltage, power, and efficiency constitute the largest difference between Lots #1 and 2. The breakdown voltages of these two lots are 115 and 128 V, respectively. The efficiency increases linearly and then flattens in the range of maximum operating current.

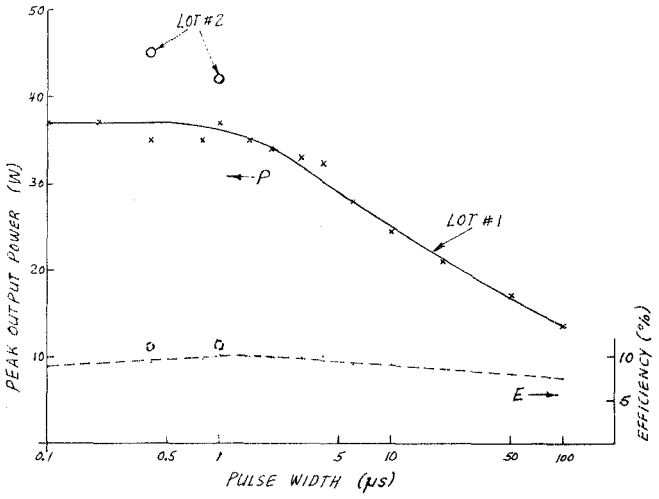

Fig. 4. Pulsed power and efficiency versus pulsewidth at $\Delta Tj < 200°C$ with 10-percent duty cycle, $f0 = 9.7$ GHz.

The peak output power is plotted in Fig. 4 versus pulsewidth in the range from 0.1 to 100 μs. The test condition is that the junction temperature-rise not exceed 200°C. The measurements were made with a duty cycle of 10 percent. The efficiencies range from 7.5 to 10.2 percent for Lot #1 and up to 11.2 percent for Lot #2.

Using Fig. 4 in conjunction with Fig. 3, operating conditions from 0.1- to 100-μs pulsewidth can be closely predicted. For example, Fig. 4 shows 25-W output power with a pulsewidth of 10 μs, while Fig. 3 reveals operating current (1.83 A), efficiency (9.5 percent), operation voltage (147 V), and ΔTj average (130°C).

IV. Conclusion

High peak pulse power (in excess of 45 W) from a single-chip silicon double-drift IMPATT diode was demonstrated. With some improvements in the thermal properties, process, and optimization of the epitaxial parameters, a minimum of 40-W peak power 10-percent duty-factor device could be made commercially available.

Acknowledgment

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